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BRINKS HOFER GILSON & LIONE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of: Lee et al.

Appln. No.: 09/748,589

Filed: December 22, 2000

For: Three-Dimensional Memory Device with ECC Circuitry

Attorney Docket No: 10519-9

Examiner: G. Portka

Art Unit: 2188

Commissioner for Patents
P. O. Box 1450
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Respectfully submitted,

6/23/04
Date

Joseph F. Hetz (Reg. No. 41,070)

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Name of Applicant, Assignee or Registered Representative

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Our Case No. 10519-9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		Examiner:	G. Portka
	Lee et al.		
Serial No.:	09/748,589	Group Art Unit:	2188
Filed:	December 22, 2000		
For:	Three-Dimensional Memory Device with ECC Circuitry		

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This Appeal is in response to the Final Office Action mailed February 2, 2004.

TABLE OF CONTENTS

I. Real Party in Interest

Matrix Semiconductor, Inc. is the real party in interest.

II. Related Appeals and Interferences

There are no related appeals or interferences that may directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1-125 have been cancelled, and Claims 126-141 are pending. Claims 126-141 have been rejected, and Claims 126, 130, and 135 have been objected to. Claims 126-141 are the subject of this appeal.

IV. Status of Amendments

No amendments have been filed subsequent to the final rejection.

V. Summary of Invention

The claimed invention relates generally to error checking and correcting (ECC) functionality and a three-dimensional memory array. The recited three-dimensional memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another. The memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers (page 3, lines 14-28). The memory cells can comprise write-once memory cells (page 4, lines 8-13) and can be selected from the group consisting of semiconductor-transistor-technology-based memory cells, magnetic-based memory cells, and organic-electronics-based memory cells, although any suitable type of memory cell can be used (page 7, line 25 – page 8, line 3).

In some embodiments, the memory array is carried by a support element that also carries ECC circuitry. With these embodiments, a housing can be provided to protect the ECC circuitry

and the memory array. In operation, at least one data bit to be stored in the memory array is received, and the ECC circuitry generates at least one ECC bit based on the at least one data bit. The at least one data bit and the at least one ECC bit are stored in the memory array. The at least one data bit and the at least one ECC bit in the memory array can be retrieved, and the ECC circuitry can identify an error in the retrieved at least one data bit and at least one ECC bit (page 7, line 1 – page 9, line 12).

In other embodiments, the ECC functionality is not in the memory device that comprises the memory array but is in a data storage system to which the memory device is adapted to be releasably coupled. The ECC functionality can be implemented in software or hardware in the data storage system or in a file system in the data storage system (page 7, lines 9-13). The memory device can comprise a housing protecting the memory array.

VI. Issues

The following issues are presented in this appeal:

1. Whether Claims 126 and 130 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 6,208,545 to Leedy in view of U.S. Patent No. 5,835,396 to Zhang or U.S. Patent No. 6,034,882 to Johnson et al.;

2. Whether Claim 135 is unpatentable under 35 U.S.C. § 103(a) over Leedy in view of Zhang or Johnson et al.;

3. Whether Claim 136 is unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 5,708,667 to Hayashi in view of Leedy and further in view of Zhang or Johnson et al.;

4. Whether Claim 137 is unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 6,321,358 to Anderson in view of Leedy and further in view of Zhang or Johnson et al.;

5. Whether Claim 138 is unpatentable under 35 U.S.C. § 103(a) over Leedy in view of Zhang or Johnson et al.; and

6. Whether Claims 126, 130, and 135 require amendment.

VII. Grouping of Claims

The rejected claims do not stand and fall together. Accordingly, Applicants identify the grouping of the claims as follows:

Group I: Claims 126-134.

Group II: Claims 135 and 139-141

Group III: Claim 136

Group IV: Claim 137

Group V: Claim 138

VIII. Argument

A. Group I Is Patentable over the Applied References

Claims 126 and 130 are the two independent claims in Group I. Claim 126 recites ECC circuitry comprising (1) ECC circuitry carried by a support element and (2) a memory array carried by the support element. The memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another, wherein the memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers. Claim 130 recites a method for using the ECC circuitry and memory array. In the Office Action, Claims 126 and 130 were rejected under 35 U.S.C. § 103(a) over Leedy in

view of Zhang or Johnson et al. The Examiner has admitted that Leedy fails to teach the recited memory array[1] and relied on the memory arrays disclosed in Zhang or Johnson et al. to cure this deficiency. However, Applicants respectfully submit that one skilled in the art would not have been motivated to make the combination proposed in the Office Action.

As stated in MPEP 2143.01, "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention ***where there is some teaching, suggestion, or motivation to do so***" (emphasis added). As also stated in MPEP 2143.01, the required teaching, suggestion, or motivation is not present when the proposed modification changes the principle of operation of a reference. In explaining this requirement, MPEP 2143.01 discusses *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). In that case, the proposed combination required that a disclosed rigid member be replaced with a resilient member. The court reversed the obviousness rejection holding that there was no suggestion to make the proposed combination because it would require a substantial reconstruction and redesign of the elements in one of the references as well as a change in the basic principle under which the element in the reference was designed to operate.

The present situation is similar to *In re Ratti*, in which the court reversed the obviousness rejection. Like the proposed combination in *In re Ratti*, the proposed combination in the present rejections requires substantial reconstruction and redesign to one of the references in the proposed combination. Leedy discloses a memory device that uses ECC and a stack of individual integrated circuits assembled after manufacturing. The primary focus of Leedy is the

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[1] See page 3 of the August 5, 2003 Office Action ("the three dimensional circuit [in Leedy] is constructed ***by bonding*** multiple substrate layers using thermal diffusion metal bonding" (emphasis added). *Cf.* Claims 126 and 130 ("wherein the memory cell layers are deposited, patterned, and etched ***without using any bonding material*** between the memory cell layers") (emphasis added).

stacked integrated circuit memory, with ECC being merely an ancillary feature. To yield the claimed invention, Leedy's stack of individual integrated circuits would be replaced with a monolithic structure in which memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers. This would require transforming Leedy's post-manufacturing assembly process in which individual integrated circuits are stacked and bonded together to an "in-situ" manufacturing process that forms a three-dimensional monolithic structure. Applicants respectfully submit that such a modification would require a substantial reconstruction and redesign to Leedy's memory array and manufacturing process and, thereby, would change the basic operating principle disclosed in Leedy.

Further, Leedy teaches away from the proposed combination by repeatedly distinguishing his stacked memory structure from a monolithic structure:

> The present invention furthers, among others, the following objectives: 1. Several-fold lower fabrication cost per megabyte of memory ***than circuits conventionally made solely with monolithic circuit integration methods***. Col. 2, lines 48-52 (emphasis added).

> This is significantly less ***than that presently experienced in monolithic DRAM circuit designs*** where the percentage of non-memory cell area can exceed 40%. Col. 6, lines 8-11 (emphasis added).

> The 3DS memory device decouples control functions ***that normally would be found adjacent the memory cells of monolithic memory circuits*** and segregates them to the controller circuit. Col. 6, lines 14-17 (emphasis added).

In summary, Applicants respectfully submit that one skilled in the art would not have been motivated to combine Leedy with Zhang or Johnson et al.[2] Without the required

[2] In the Office Action, it was argued that it would have been obvious to add ECC circuitry to the memory arrays disclosed in Zhang and Johnson et al. so that they could benefit from error-correction capabilities. Applicants respectfully disagree. ECC circuitry adds delays and increases chip size, which is often undesirable in high-density memories that try to maximize the ratio of number of memory cells/chip size. Accordingly, Applicants respectfully submit that one skilled in the art would have followed conventional wisdom and ***not*** have added ECC circuitry to the memory arrays disclosed in Zhang and Johnson et al.

motivation, an obviousness rejection is nothing more than hindsight reconstruction using the claims as a blueprint to pick and choose isolated elements found in various prior art references. Accordingly, Applicants respectfully request that the rejections of independent Claims 126 and 130 and their dependent claims be withdrawn.

B. Group II Is Patentable over the Applied References

Claim 135 is the one independent claim in Group II and recites a data storage system comprising ECC functionality and a memory device adapted to be releasably coupled to the data storage system. The memory device comprises a memory array comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another, wherein the memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers. Claim 135 was rejected under 35 U.S.C. § 103(a) over Leedy in view of Zhang or Johnson et al. However, Applicants respectfully submit that the proposed combination of Leedy and either Zhang or Johnson et al. does not teach each and every element recited in Claim 135.[3]

As shown in Figure 2c, Leedy teaches the use of ECC circuitry in a memory controller circuit ***in the memory device — not in a data storage system***, as recited in Claim 135. With respect to Zhang and Johnson et al., there is no teaching whatsoever in either of those references of any type of ECC functionality, much less ECC functionality in a data storage system. Because none of the references in the proposed combination teaches ECC functionality in a data storage system, Applicants respectfully submit that the 35 U.S.C. § 103(a) rejections of independent Claim 135 and its dependent claims should be withdrawn.

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[3] Even if the proposed combination of Leedy and either Zhang or Johnson et al. taught all of the elements in Claim 135, Applicants respectfully submit that the rejections should still be withdrawn since there is no suggestion to combine Leedy with either Zhang or Johnson et al., as discussed in the previous section.

Applicants further note that there is no suggestion to move the ECC circuitry from the memory device to the data storage system. Col. 6, lines 61-64 list ECC circuitry among components that are conventionally part of a memory device, such as address decoders, gate-line and DRAM layer select logic, and refresh and self-test logic. Since Leedy listed the ECC circuitry among components that are conventionally part of a memory device, one skilled in the art would no sooner move the ECC circuitry from the memory device to the data storage system as he would move the address decoders or listed components to the data storage system.

C. Group III Is Patentable over the Applied References

Group III contains dependent Claim 136, which recites that the ECC functionality is implemented in software in a data storage system. Claim 136 was rejected under 35 U.S.C. § 103(a) over Hayashi in view of Leedy and further in view of Zhang or Johnson et al. In the Office Action, it was admitted that neither Leedy, Zhang, nor Johnson et al. teaches ECC functionality implemented in software. Hayashi was used in an attempt to cure this deficiency. However, while Hayashi teaches implementing ECC functionality in software, Hayashi does not teach implementing ECC functionality in software ***in a data storage system***, as recited in Claim 136. Figure 2 in Hayashi shows a host (or data storage system) coupled with a memory device 100. As described at col. 4, lines 26-25, it is the CPU 102 or the controller LSI 101 of the memory device 100 — not of the host/data storage system — that contains the ECC functionality.

Because none of the applied references in the proposed combination teaches ECC functionality implemented in software in a data storage system, Applicants respectfully submit that the 35 U.S.C. § 103(a) rejection of Claim 136 should be withdrawn.

D. Group IV Is Patentable over the Applied References

Group IV contains dependent Claim 137, which recites that the ECC functionality is implemented in a file system in a data storage system. Claim 137 was rejected under 35 U.S.C. § 103(a) over Anderson in view of Leedy and further in view of Zhang or Johnson et al. In the Office Action, it was admitted that neither Leedy, Zhang, nor Johnson et al. teaches ECC functionality implemented in a file system. However, it was asserted that Figure 31 and the accompanying text in Anderson cures this deficiency. Applicants respectfully disagree. Col. 22, lines 64-66 states that "FIG. 31 is a block diagram illustrating how file system information ***is combined with, or embedded in,*** ECC information prior to recording the information on the disc." (emphasis added). Since file system information is combined with or embedded in ECC information, it is clear that the file system information and the ECC information are separately generated. Accordingly, the ECC functionality is not implemented in a file system, as recited in Claim 137. For this reason, Applicants respectfully submit that the 35 U.S.C. § 103(a) rejection of Claim 137 should be withdrawn.

E. Group V Is Patentable over the Applied References

Group V contains dependent Claim 138, which recites that the ECC functionality is implemented in hardware in a data storage system. It appears that the ECC circuitry in Leedy was asserted to correspond to the recited hardware implementation of ECC functionality. However, Claim 138 does not merely require the ECC functionality to be implemented in hardware. It requires that the ECC functionality be implemented in hardware ***in a data storage system***. As described above, the ECC circuitry in Leedy is in a memory device — not in a data storage system. Accordingly, the proposed combination fails to teach each and every element

recited in Claim 138. For this reason, Applicants respectfully submit that the 35 U.S.C. § 103(a) rejection of Claim 138 should be withdrawn.

F. Claims 126, 130, and 135 Do Not Require Amendment

Claims 126, 130, and 135 were objected to for an informality and were asserted to require amendment. Specifically, it was noted that the recitation of a memory array comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another does not require (1) a plurality of arrays, each being a layer or (2) that a cell makes up a layer. It was suggested that the claims be amended to preclude the interpretation that each cell can contain plural layers within itself.

Applicants respectfully submit that the language in these claims is clear and does not require amendment. Claims 126, 130, and 135 recite that "the memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another." Claims 126, 130, and 135 call for "a" memory array, and there is no need to recite a plurality of arrays. Additionally, Claims 126, 130, and 135 are silent as to the makeup of the individual memory cells, and there is no need to recite whether or not a cell makes up a layer or whether each cell contains plural layers within itself.

In summary, Claims 126, 130, and 135, as written, particularly point out and distinctly claim the subject matter that Applicants regard as their invention. Accordingly, Applicants respectfully submit that Claims 126, 130, and 135 do not contain informalities that require amendment.

IX. Conclusion

For the reasons set forth above, Applicants respectfully submit that all rejections and objections should be removed and that Claims 126-141 should be passed to allowance.

Dated: June 23, 2004

Respectfully submitted,

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X. Appendix

126. A three-dimensional memory device with ECC circuitry comprising:

a support element;

error checking and correcting (ECC) circuitry carried by the support element; and

a memory array carried by the support element, wherein the memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another, wherein the memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers.

127. The invention of Claim 126 further comprising a housing protecting the error checking and correcting (ECC) circuitry and the memory array.

128. The invention of Claim 126, wherein the memory cells comprise write-once memory cells.

129. The invention of Claim 126, wherein the memory cells are selected from the group consisting of semiconductor-transistor-technology-based memory cells, magnetic-based memory cells, and organic-electronics-based memory cells.

130. A method for storing data and error checking and correcting (ECC) bits in a three-dimensional memory device with ECC circuitry, the method comprising:

(a) providing a three-dimensional memory device with ECC circuitry to a data storage system, the memory device comprising:

a support element;

error checking and correcting (ECC) circuitry carried by the support element; and

a memory array carried by the support element, wherein the memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another, wherein the memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers;

(b) with the memory device, receiving at least one data bit to be stored in the memory array;

(c) with the ECC circuitry, generating at least one ECC bit based on the at least one data bit; and

(d) storing the at least one data bit and the at least one ECC bit in the memory array.

131. The invention of Claim 130 further comprising:

(e) retrieving the at least one data bit and the at least one ECC bit in the memory array; and

(f) with the ECC circuitry, identifying an error in the retrieved at least one data bit and at least one ECC bit.

132. The invention of Claim 130, wherein the memory device further comprises a housing protecting the error checking and correcting (ECC) circuitry and the memory array.

133. The invention of Claim 130, wherein the memory cells comprise write-once memory cells.

134. The invention of Claim 130, wherein the memory cells are selected from the group consisting of semiconductor-transistor-technology-based memory cells, magnetic-based memory cells, and organic-electronics-based memory cells.

135. A system for storing an error checking and correcting (ECC) bit in a three-dimensional memory array, the system comprising:

a data storage system; and

a memory device adapted to be releasably coupled to the data storage system, the memory device comprising a memory array carried by the support element, wherein the memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another, wherein the memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers;

wherein the data storage system comprises error checking and correcting (ECC) functionality.

136. The invention of Claim 135, wherein the ECC functionality is implemented in software in the data storage system.

137. The invention of Claim 135, wherein the ECC functionality is implemented in a file system in the data storage system.

138. The invention of Claim 135, wherein the ECC functionality is implemented in hardware in the data storage system.

139. The invention of Claim 135, wherein the memory device further comprises a housing protecting the memory array.

140. The invention of Claim 135, wherein the memory cells comprise write-once memory cells.

141. The invention of Claim 135, wherein the memory cells are selected from the group consisting of semiconductor-transistor-technology-based memory cells, magnetic-based memory cells, and organic-electronics-based memory cells.